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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,913	09/24/2003	Hwa Jeong Lee	CU-3369 RJS	5770

26530 7590 12/27/2006

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/669,913	LEE ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 31 October 2006. Claims 1-4 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogan (US 6,750,839).

Regarding claim 1, Hogan discloses a liquid crystal display device comprising:

an analog voltage signal generator (Figure 1 shows Controller 34, Serial Interface 36, VP REG, VN REG, Digital MUX 30, DACs 28 and the buffer circuits as an analog voltage signal generator.) storing an input synchronous signal and a plurality of input digital data signals (Figure 1 shows VN REG and VP REG which store a plurality of input digital data signals, and since it is stated in column 3, lines 49-54 that the controller switches the MUX 30 between VP and VN in SYNCHRONIZATION with signal VCOM, then there would inherently be a synchronous signal.), and converting the stored digital data signals into a plurality of analog voltage signal pairs (Figure 1 shows that the DACs 28 each convert the data stored either in the VN REG or the VP REG from digital signals into analog signals, where the pairs consist of V0 and V1, V1 and V2, V2 and V3, V3 and V4 and V4 and V5.);

a plurality of reference voltage generators for dividing a boosted source voltage according to the analog voltage signal pairs from the analog voltage signal generator to generate a plurality of reference voltages (Figure 1 shows a plurality of reference voltage generators, with a first reference voltage generator consisting of the resistors between reference voltages V0 and V1, a second reference voltages generator consisting of the resistors between reference voltages V1 and V2, and so on.); and

a source driver circuit (Figure 1 shows the select registers and MUX 1 and MUX 2 for driving source lines C1 and C2.) for receiving the plurality of reference voltages from the plurality of reference voltage generators (Figure 1 shows that MUX 1 and MUX 2 each receive the signals from the resistor strings.), wherein a digital/analog converter of the analog voltage signal generator changes a reference voltage value and outputs a changed value reference voltage to the reference voltage generators, to thereby change a contrast ratio according to the changed reference voltage values when a command to change a reference voltage value is transferred to the digital/analog converter (Figure 1 and column 3, lines 41-64 explain that the select signal sent from line 32 to the MUX 30 decides whether the values input to the DACs will be from VN REG or VP REG, which means that each reference voltage value, V0-V4, will have a changed value outputted from the DAC based on this selection signal, and since the selection signal is sent to the MUX 30, and the value is changed and sent to the DAC, then the DAC will change the value when the change signal is sent to it, and this is done in order to achieve a change in contrast that improves the contrast as explained in column 5, lines 51-62.).

Hogan fails to teach that the registers store the input signals in response to a write enable signal and that the stored digital signals are converted into a plurality of analog voltage signal pairs in response to an output enable signal, however, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to store the input signals in response to a write enable signal and to convert the signals based on an output enable signal because it is well known in the art to do so in order to allow for the proper timing of the signals to take place.

Regarding claim 2, Hogan discloses a liquid crystal display device as claimed in claim 1, wherein the analog voltage signal generator includes:

a data storage section storing the input synchronous signal and the plurality of input digital data signals in response to the write enable signal (As explained above, VN REG and VP REG store the plurality of input digital data signals, and these values would be sent based on a write enable signal.);

the digital/analog converter converting the plurality of input digital data signals stored in the data storage section into a plurality of analog signals in response to the input synchronous signal when the output enable signal is generated (As explained above the DACs 28 will convert the digital signals into analog signals based on an output enable signal.); and

a buffer amplifier amplifying the plurality of input analog signals and outputting the plurality of analog voltage signal pairs (Figure 1 shows buffer amplifiers in between the DACs 28 and the voltage generating circuit string 20.).

Regarding claim 3, Hogan discloses a liquid crystal display device as claimed in claim 2, wherein the data storage section stores a fixed reference voltage signal pair according to voltage-transmission factor curve feature, and the digital/analog converter changes the fixed reference voltage signal pair stored in the storage section in response to an external reference voltage change command and outputs a changed reference voltage (As explained above and in column 3, lines 41-64, VN REG and VP REG store

the digital signals, which are output based on the selection signal 32 sent to the MUX 30 such that either the reference values stored in VN REG or the values stored in VP REG are output according to VCOM.).

Regarding claim 4, Hogan discloses a liquid crystal display device as claimed in claim 1, wherein the plurality of reference voltage generators include a plurality of resistors connected to each other in series between a power supply terminal and a ground terminal for generating the plurality of reference voltages (Figure 1 shows that the plurality of reference voltage generators, with a first reference voltage generator consisting of the resistors between reference voltages V0 and V1, a second reference voltages generator consisting of the resistors between reference voltages V1 and V2, and so on, each contain a plurality of resistors connected between the reference voltages.).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

13 December 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER